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A Novel Multi-Context Non-Volatile Content-Addressable Memory Cell and Multi-Level Architecture for High Reliability and Density

Xian Wang‡, Deming Zhang†,* , Kaili Zhang†,* , Erya Deng†, You Wang* and Weisheng Zhao†,*

‡School of Electronic and Information Engineering, Beihang University, Beijing 100191, China

†Fert Beijing Institute, MIIT Key Laboratory of Spintronics, School of Integrated Circuit Science and Engineering, Beihang University, Beijing 100191, China

* Hefei Innovation Research Institute, Beihang University, Hefei 230013, China

Email：zy1902302@buaa.edu.cn
deming.zhang@buaa.edu.cn

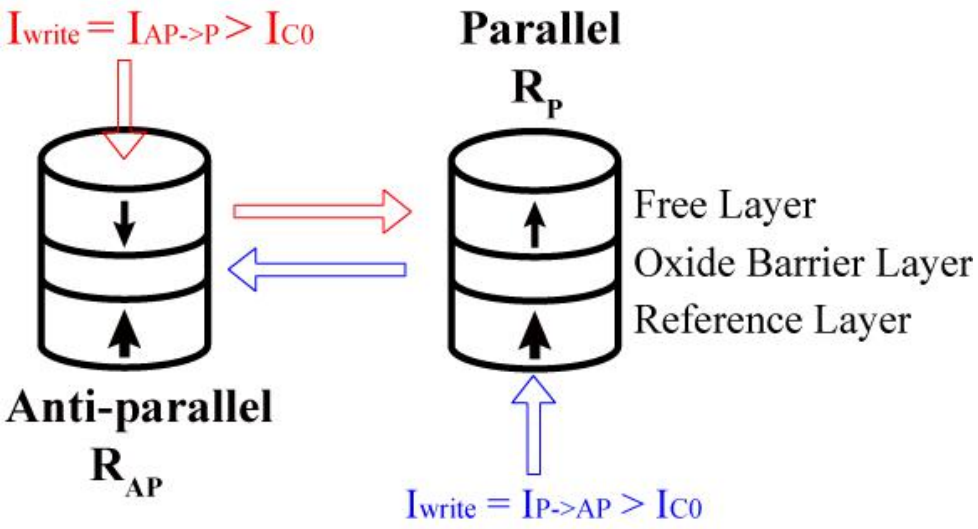
北京航空航天大學 BEIHANG UNIVERSITY

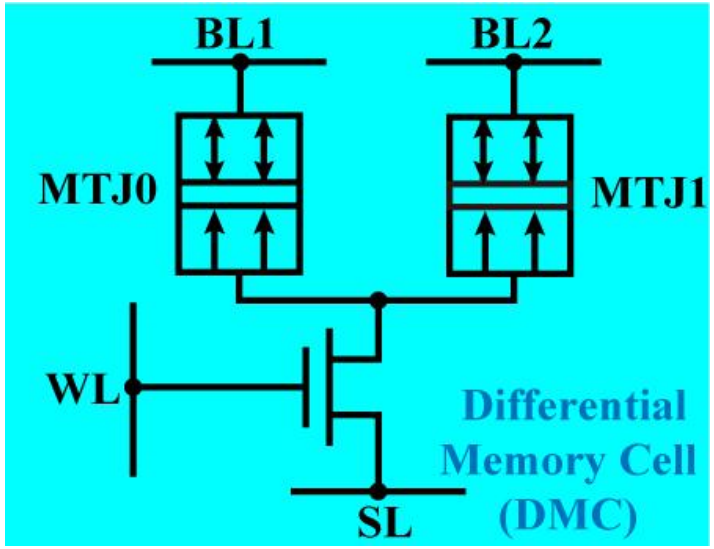
Outline

1. Introduction
2. Proposed MCC for High Reliability and Speed
3. Proposed MLA for High Reliability and Density
4. Conclusion

Outline

Introduction





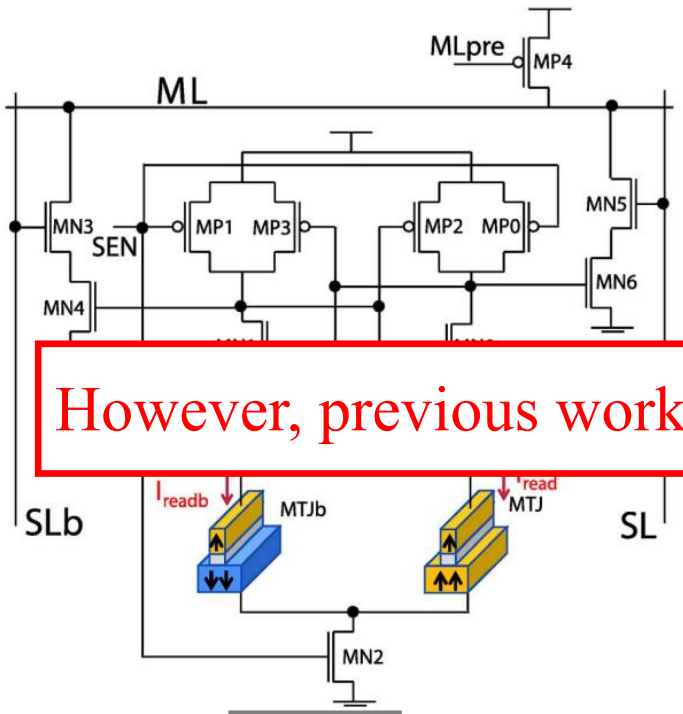
$TMR = (R_{AP} - R_P) / R_P$ (~100%, limited) → To improve sensing reliability

(a) Structure of MTJ and the STT write mechanism [1]

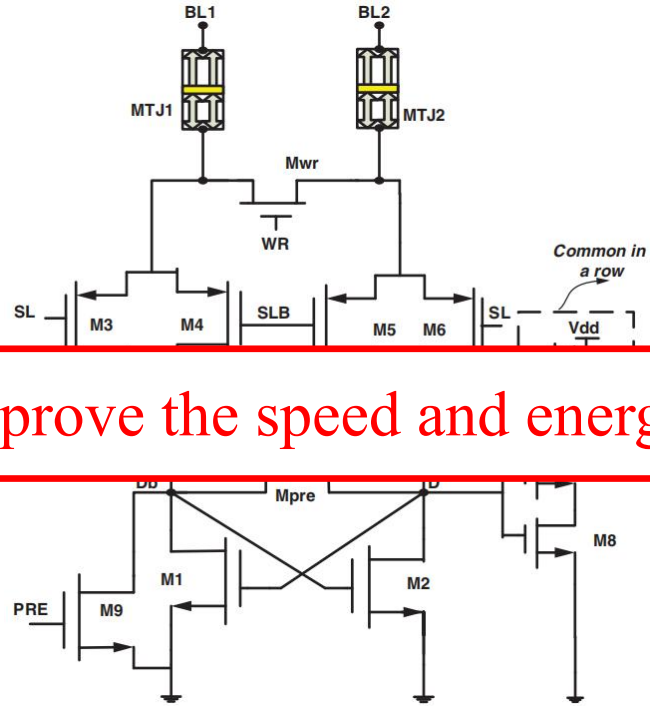
(b) The previously proposed 1T/2MTJ memory cell [2]

[1] M. Wang, W. Cai, D. Zhu, Z. Wang, J. Kan, Z. Zhao, K. Cao, Z. Wang, Y. Zhang, T. Zhang et al., "Field-free switching of a perpendicular magnetic tunnel junction through the interplay of spin–orbit and spin-transfer t orques," Nature electronics, vol. 1, no. 11, p. 582, 2018, doi: 10.1038/s41928-018-0160-7.
[2] W. Zhao, L. Torres, Y. Guillemenet, et al. Design of MRAM based logic circuits and its applications[C]//Proceedings of the great lakes symposium on Great lakes symposium on VLSI, 2011: 431-436.

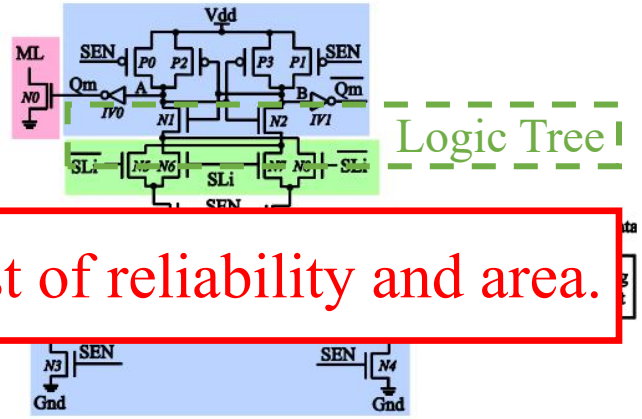
Introduction



Ref [3]



Ref [4]



Ref [5]

However, previous works improve the speed and energy at the cost of reliability and area.

[3] Y. Zhang, W. Zhao, J. Klein, D. Ravelsona and C. Chappert, “Ultra_x0002_High Density Content Addressable Memory Based on Current In_x0002_duced Domain Wall Motion in Magnetic Track,” in IEEE Transac_x0002_tions on Magnetics, vol. 48, no. 11, pp. 3219-3222, Nov. 2012, doi: 10.1109/TMAG.2012.2198876.

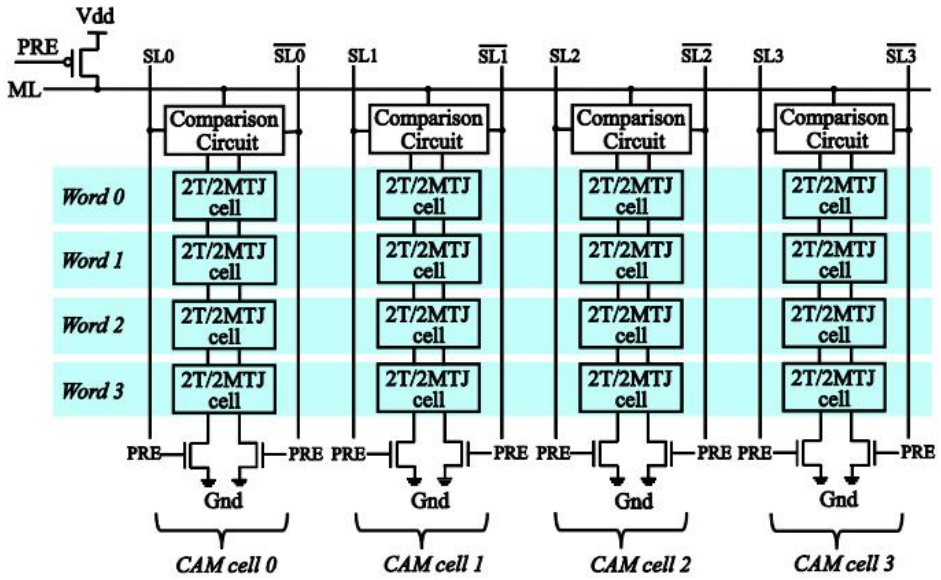
[4] A. Shaban, S. Ahmad, N. Alam and M. Hasan, “Compact and Reliable Low Power Non-Volatile TCAM Cell,” 2018 8th International Sympo_x0002_sium on Embedded Computing and System Design (ISED), pp. 100-104, 2018, doi: 10.1109/ISED.2018.8704013.

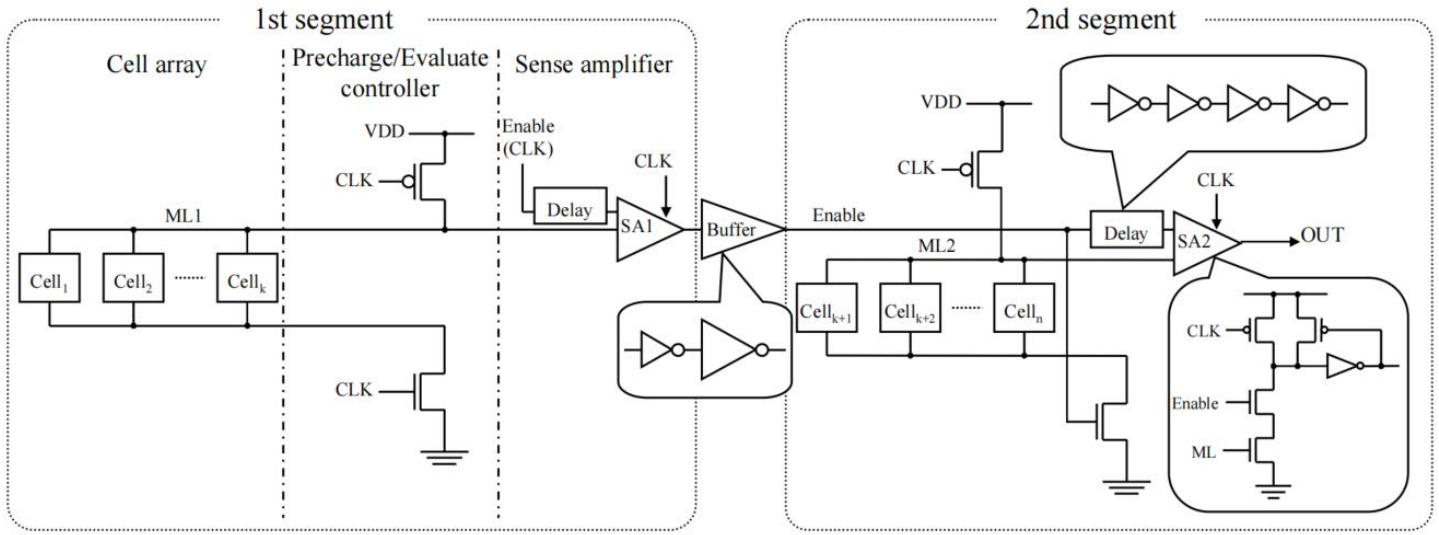
[5] E. Deng, L. Anghel, G. Prenat and W. Zhao, “Multi-context non_x0002_volatile content addressable memory using magnetic tunnel junctions,” 2016 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), pp. 103-108, 2016, doi: 10.1145/2950067.2950106.

Introduction

Large search delay

Low density and reliability.





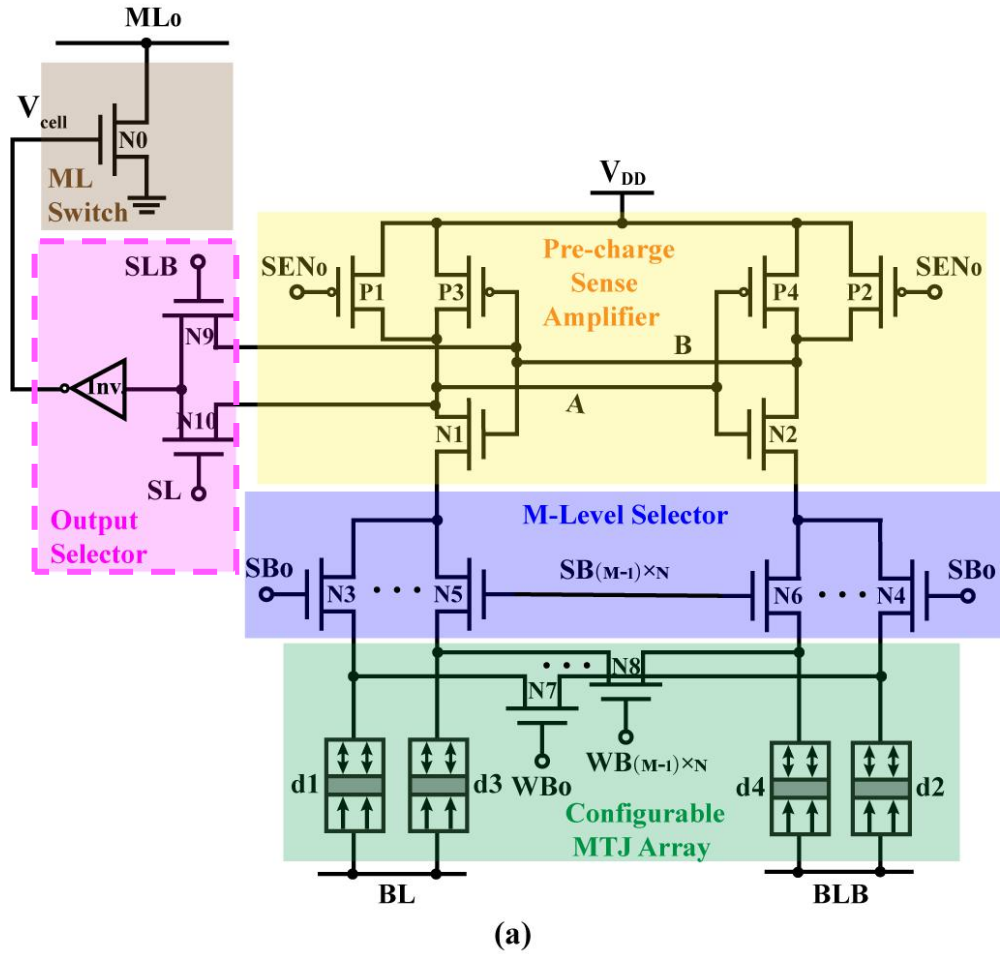
(a) Multi-context architecture [5]

(b) Segmented match-line (ML) architecture [6]

[6] S. Matsunaga, A. Katsumata, M. Natsui and T. Hanyu, “Design of a Low-Energy Nonvolatile Fully-Parallel Ternary CAM Using a Two-Level Segmented Match-Line Scheme,” 2011 41st IEEE Interna_x0002_tional Sy mposium on Multiple-Valued Logic, pp. 99-104, 2011, doi: 10.1109/ISMVL.2011.41.

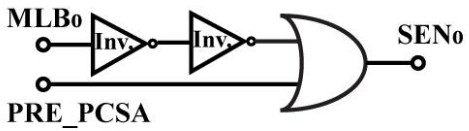
Outline

Proposed multi-context cell (MCC)



(a)

- Explanation:
  1. M denotes the amount of levels in the MLA;
  2. N denotes the amount of bits per level in the MLA;
  3. i denotes the number of bit in a word;
  4. j denotes the number of word in a NV-CAM.

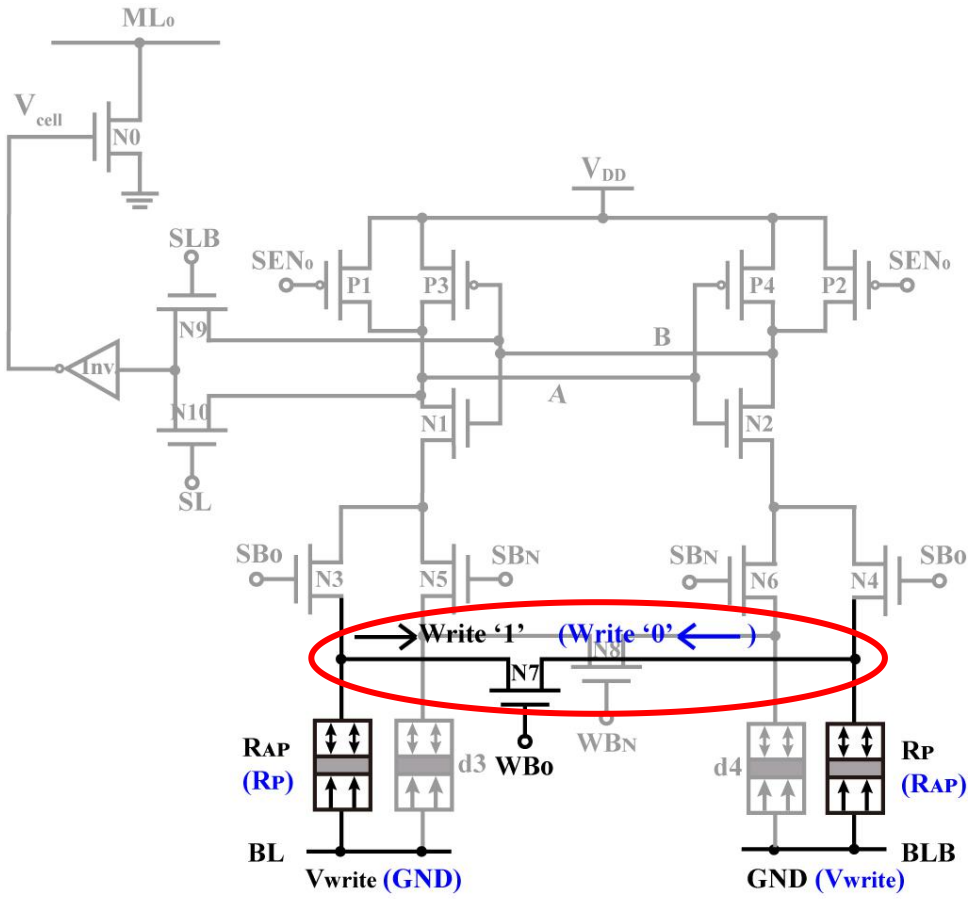


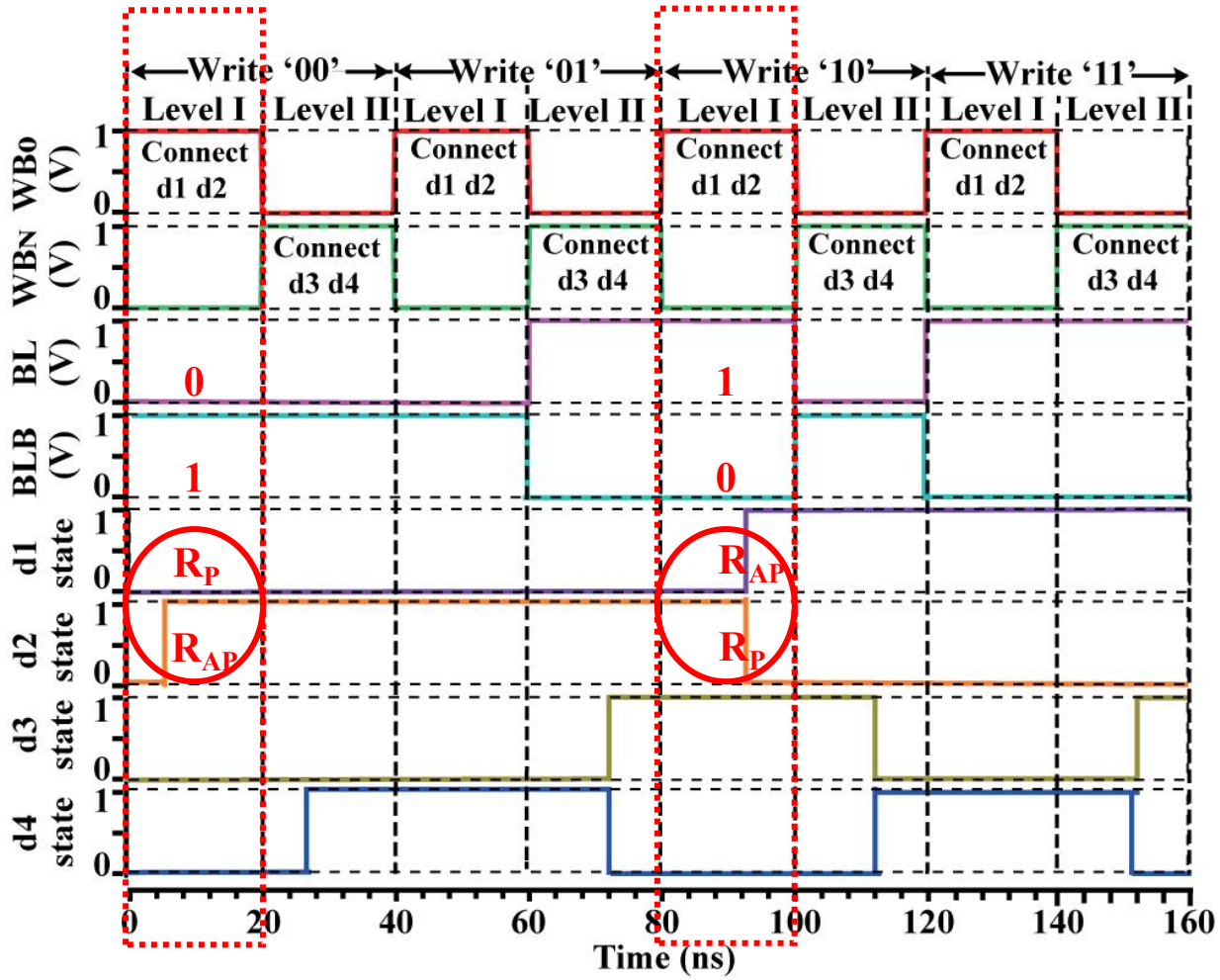
(b)

Schematic of the proposed multi-context cell (MCC) circuit and (b) the SEN generator circuit

The write operation

➢ Level I：

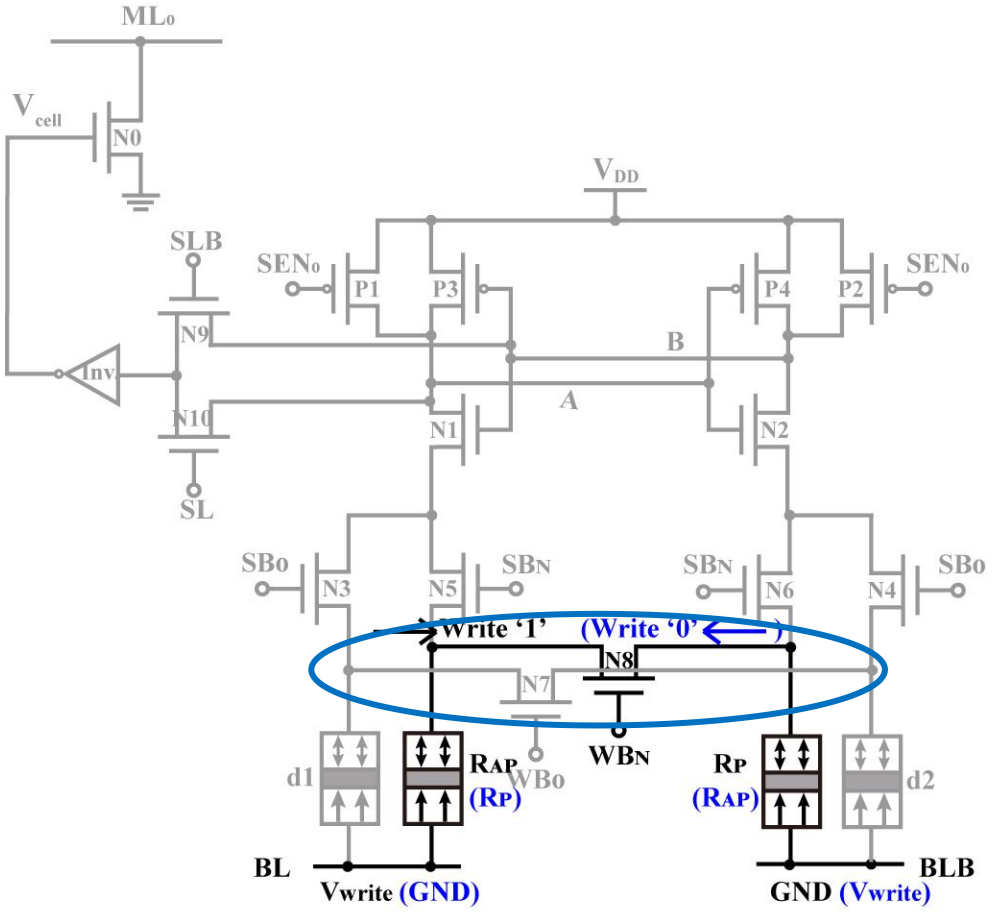


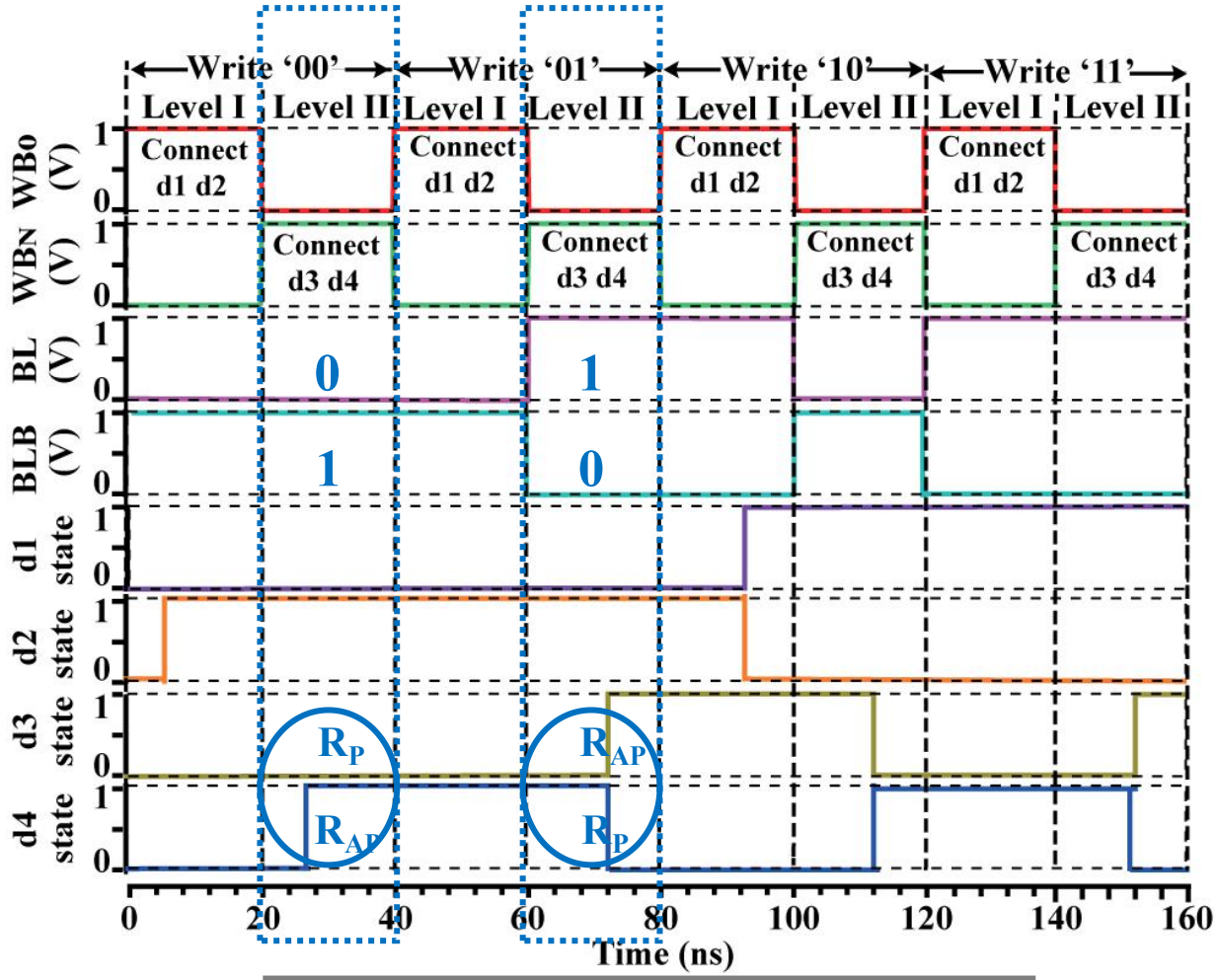


Timing diagram of the write operation

The write operation

➢ Level II：

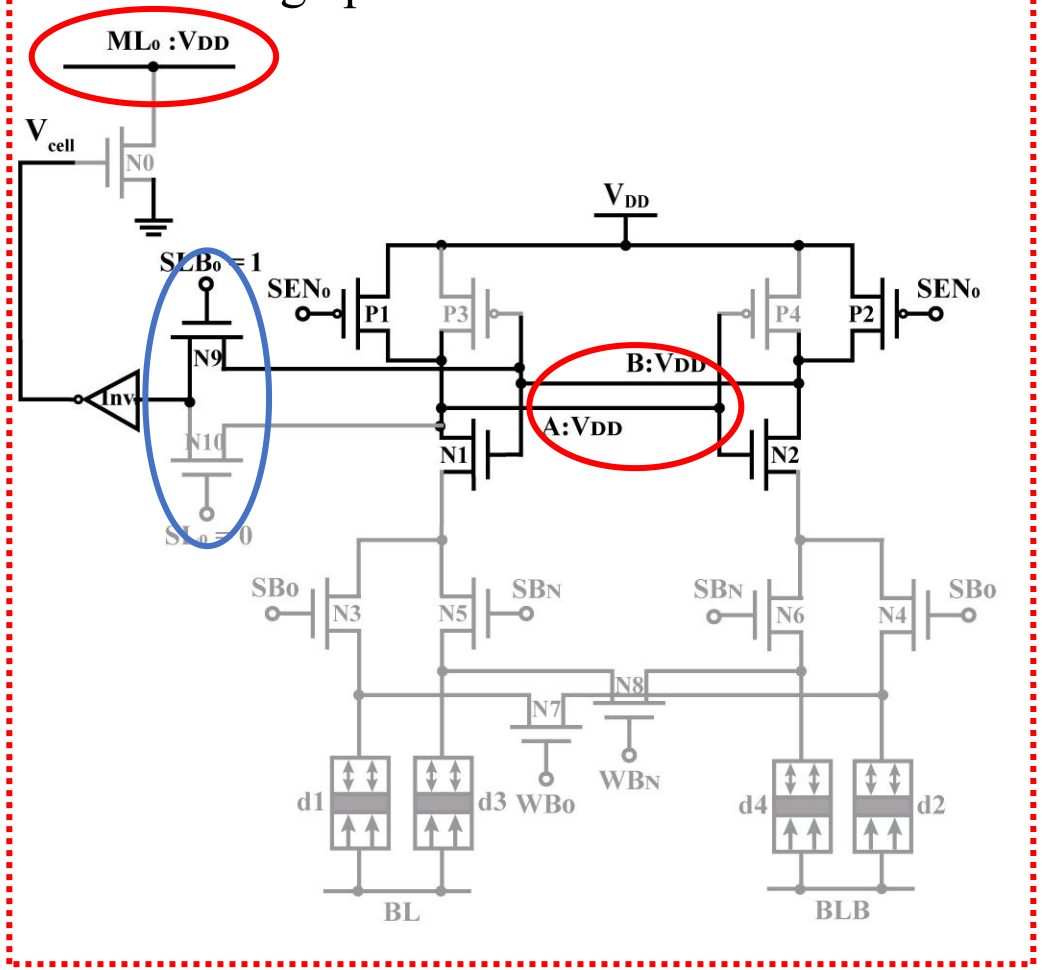


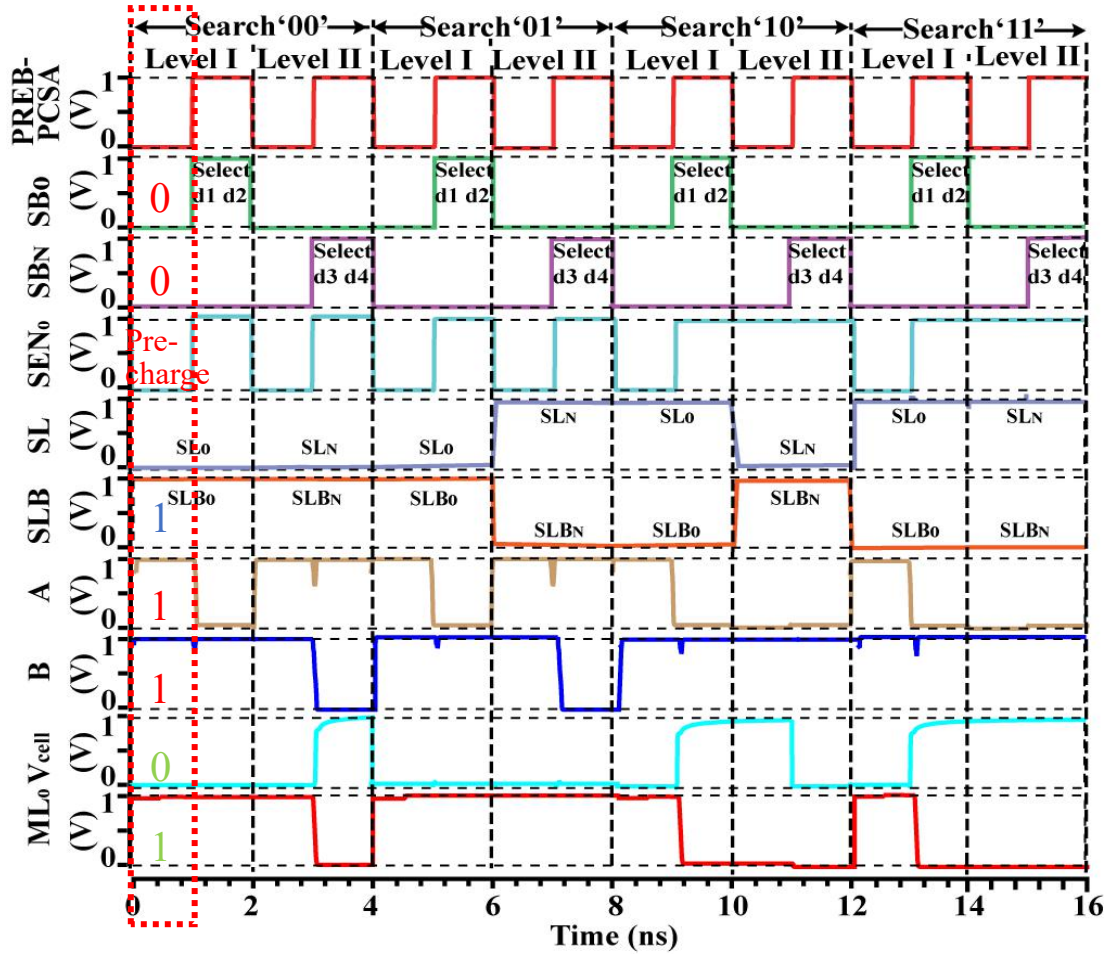


Timing diagram of the write operation

The search operation

➢ Pre-charge phase of level I：

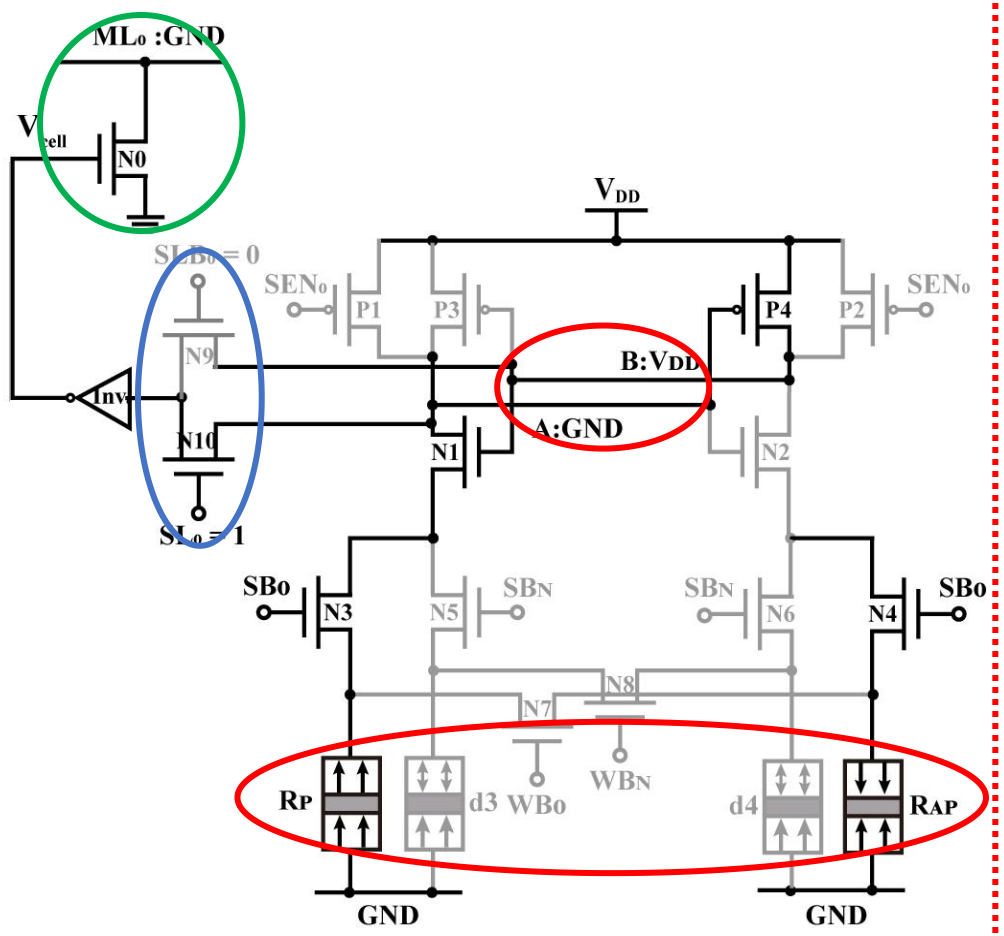


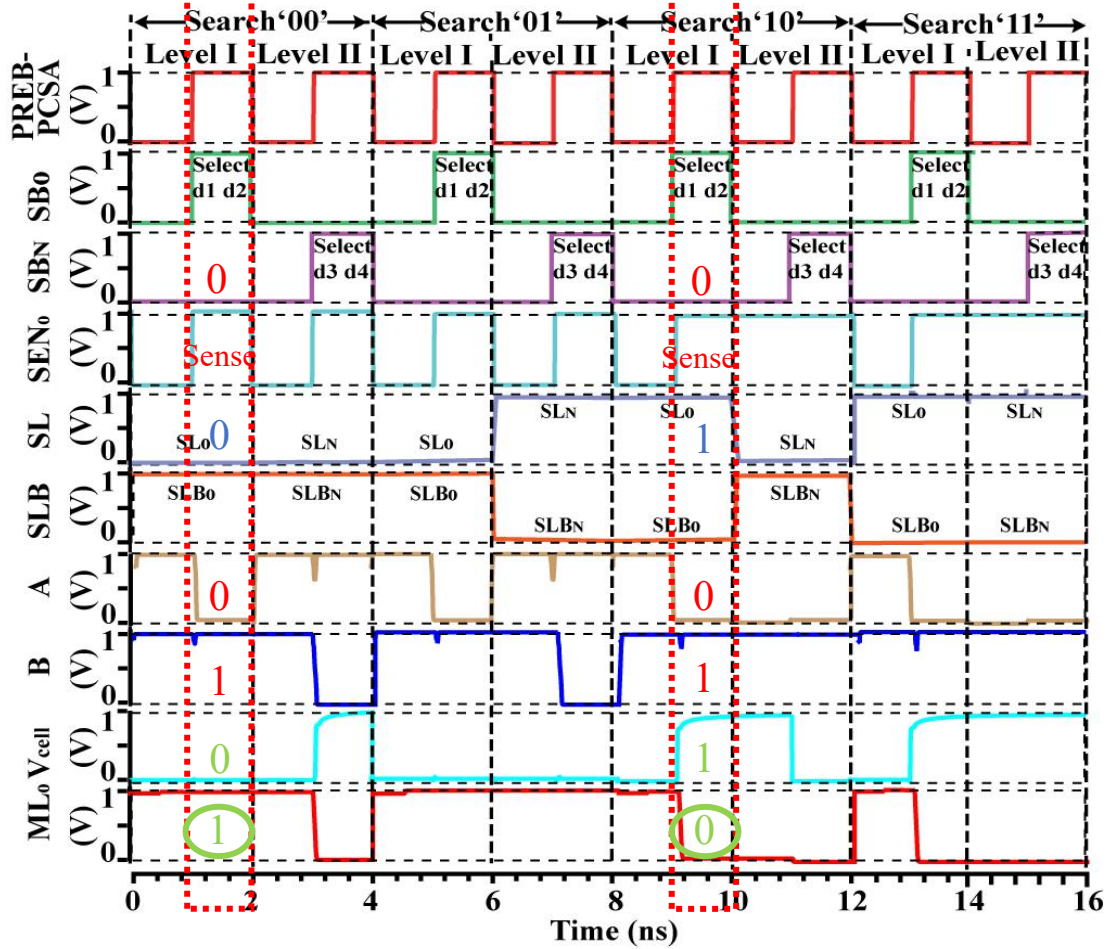


Timing diagram of the search operation

The search operation

- Sense phase of level I：

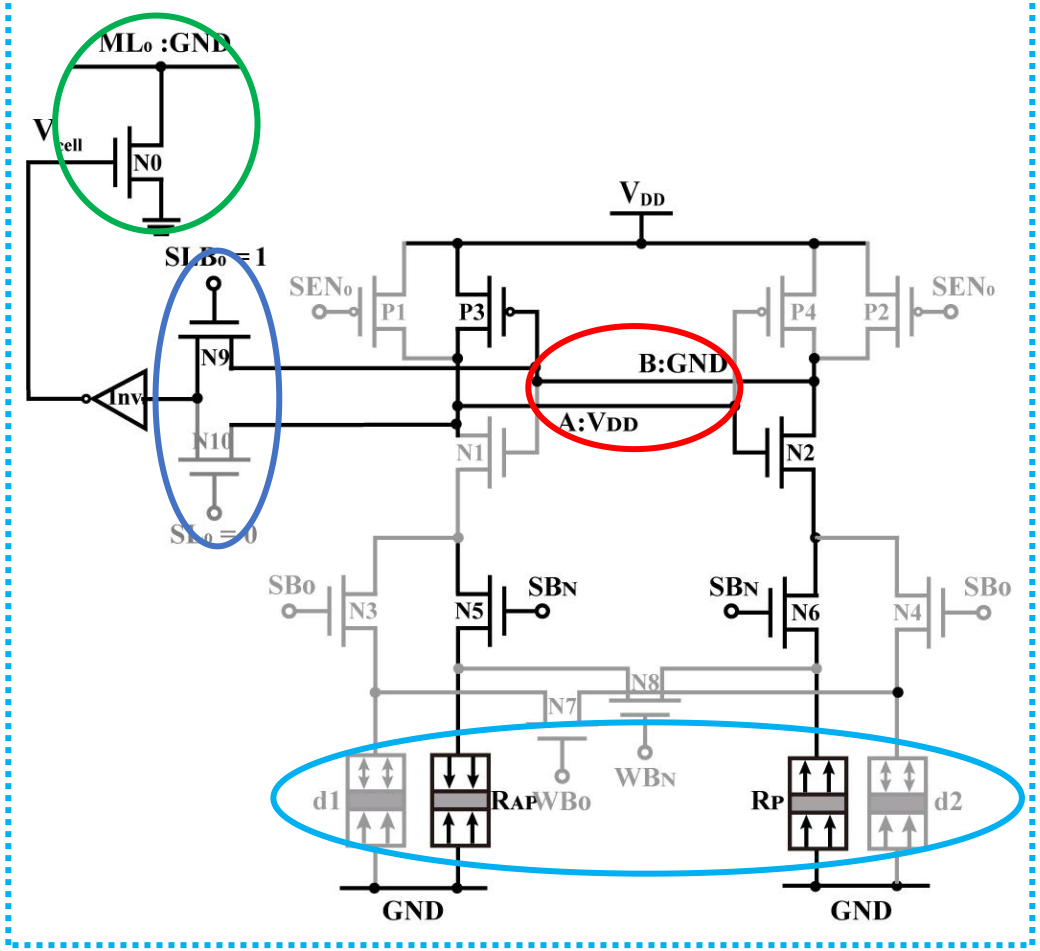


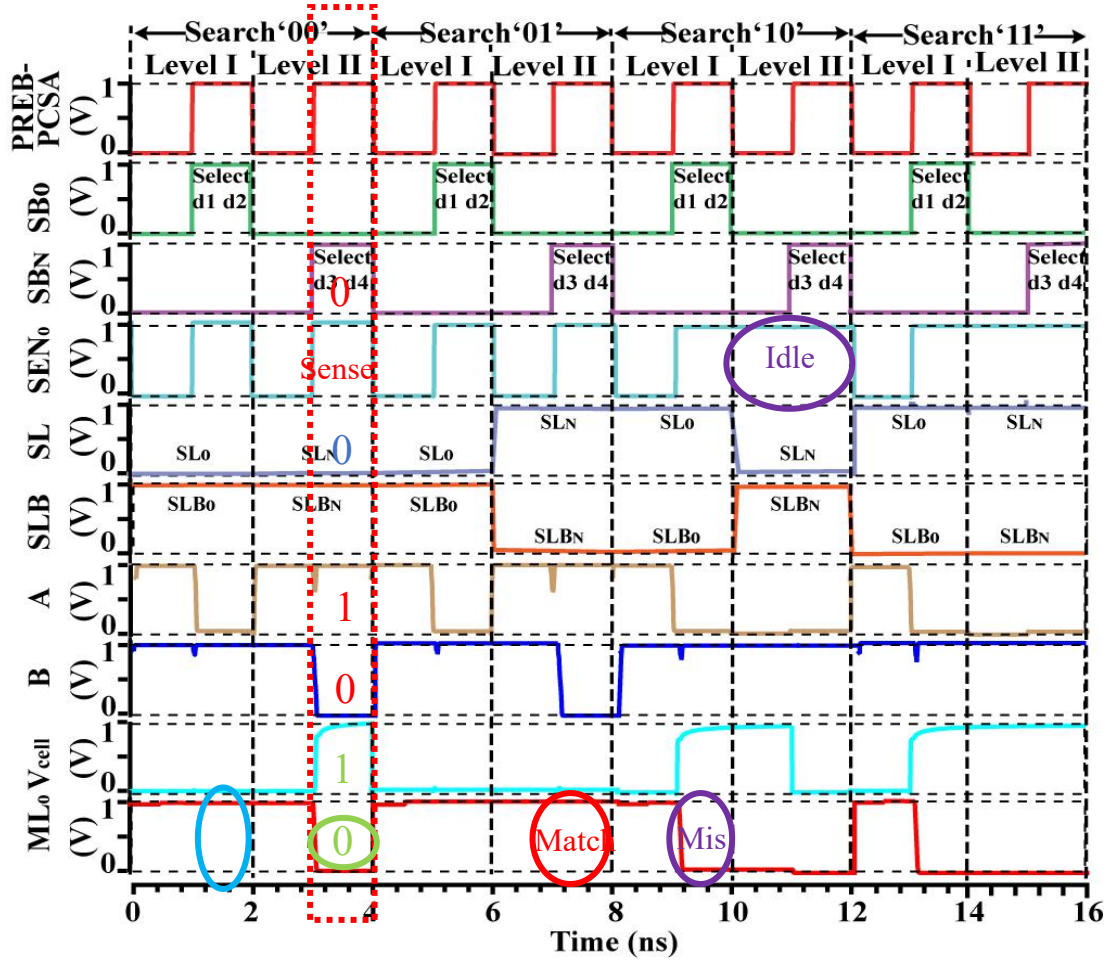


Timing diagram of the search operation

The search operation

- Sense phase of level II:





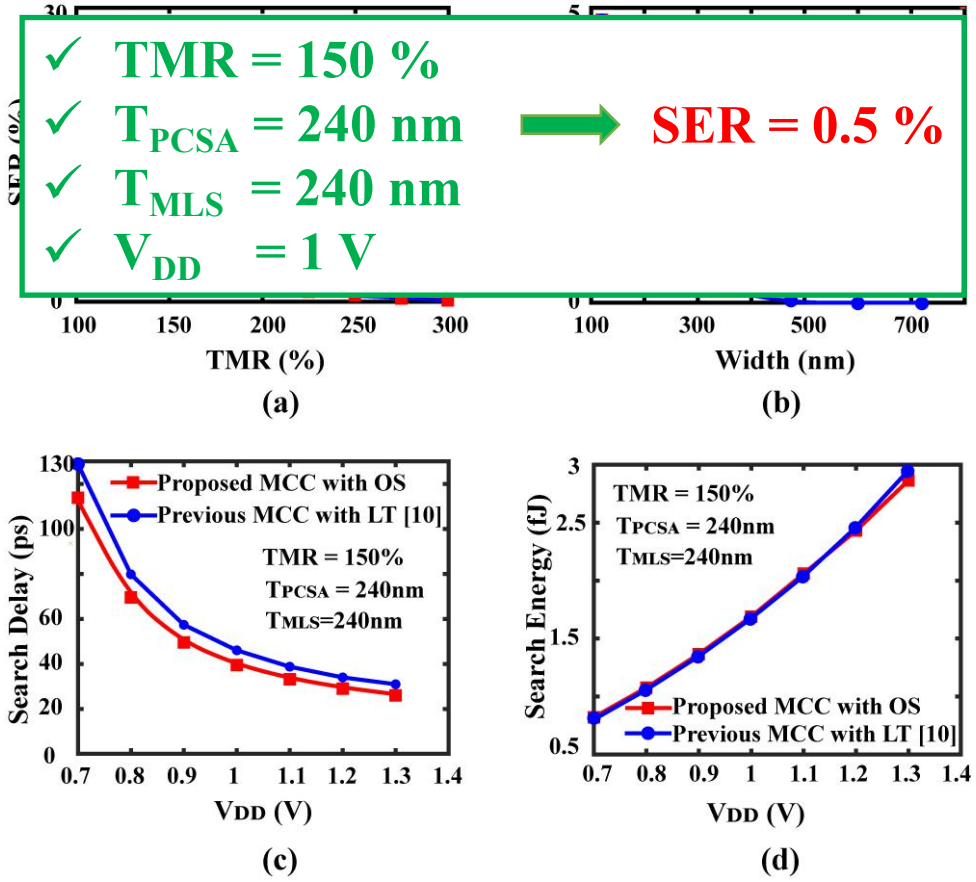
Timing diagram of the search operation

Performance Evaluation

- Simulation conditions:
  1. A physics-based STT-MTJ compact model [7];
  2. A commercial CMOS 40 nm design kit.

CRITICAL PARAMETERS FOR THE PROPOSED NV-CAM

Parameter	Description	Default Value
L	Length of the transistors	40 nm
W	Width of the transistors	120 nm
D	Diameter of MTJ nanopillar	40 nm
TMR(0)	TMR ratio at 0 V_{bias}	1.5
T_{free}	Thickness of free layer	1.3 nm
T_{oxide}	Thickness of oxide layer	0.85 nm
R·A	Resistance-area product	5 $\Omega \cdot \mu m^2$
ΔTMR	Variation of TMR ratio	0.03
ΔT_{free}	Variation of free layer thickness	0.03
ΔT_{oxide}	Variation of oxide layer thickness	0.03
a	Length of MTJ	40 nm
b	Width of MTJ	40 nm
V_{DD}	Voltage supply	1 V

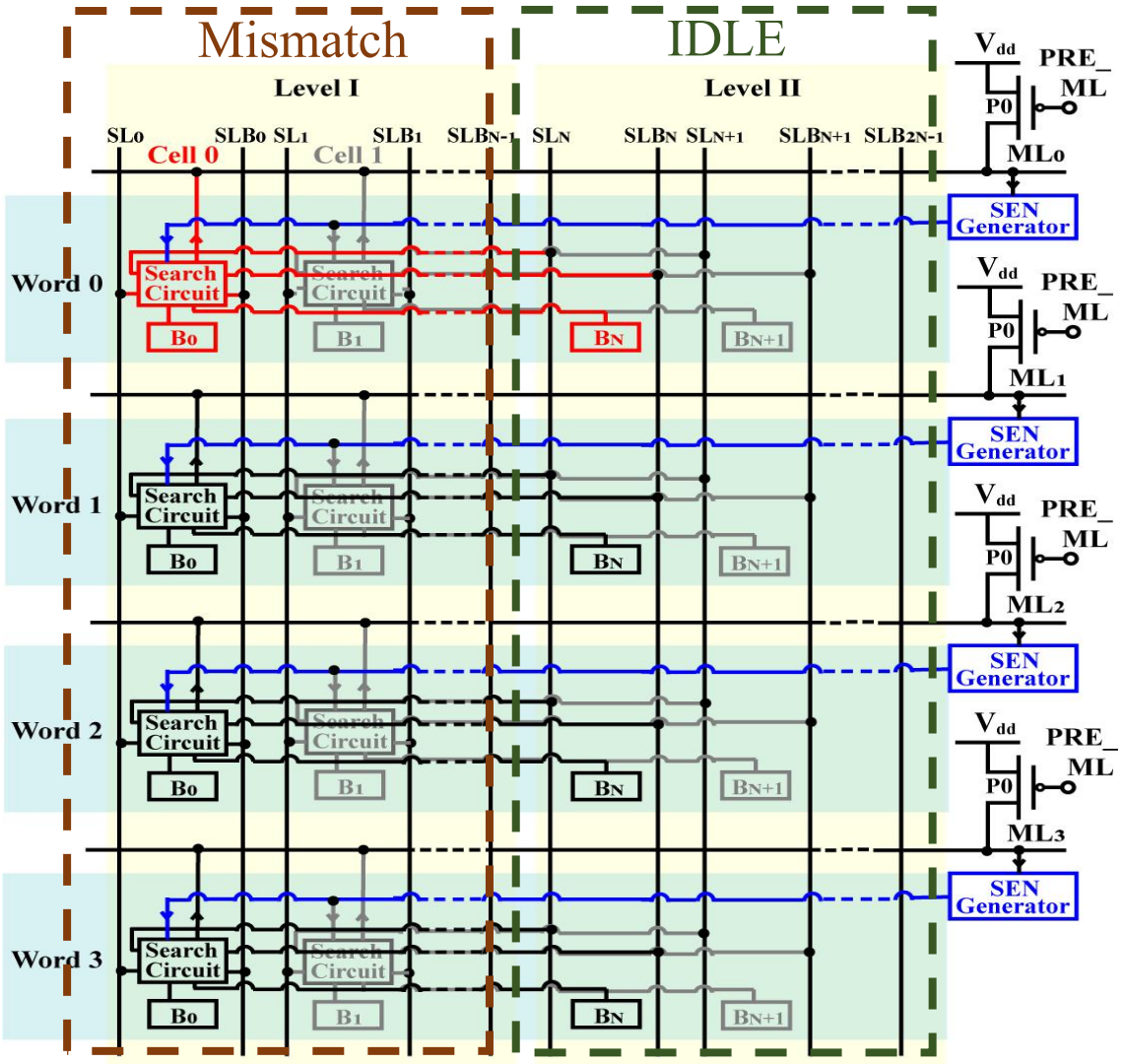


Performance graph of the proposed and previous scheme

[7] Y. Wang, Hao Cai, Lirida Alves de Barros Naviner, Yue Zhang et al., "Compact Model of Dielectric Breakdown in Spin-Transfer Torque Mag_x0002_netic Tunnel Junction," in IEEE Transactions on Electron Devices, vol. 63, no. 4, pp. 1762-1767, April 2016, doi: 10.1109/TED.2016.2533438.

Outline

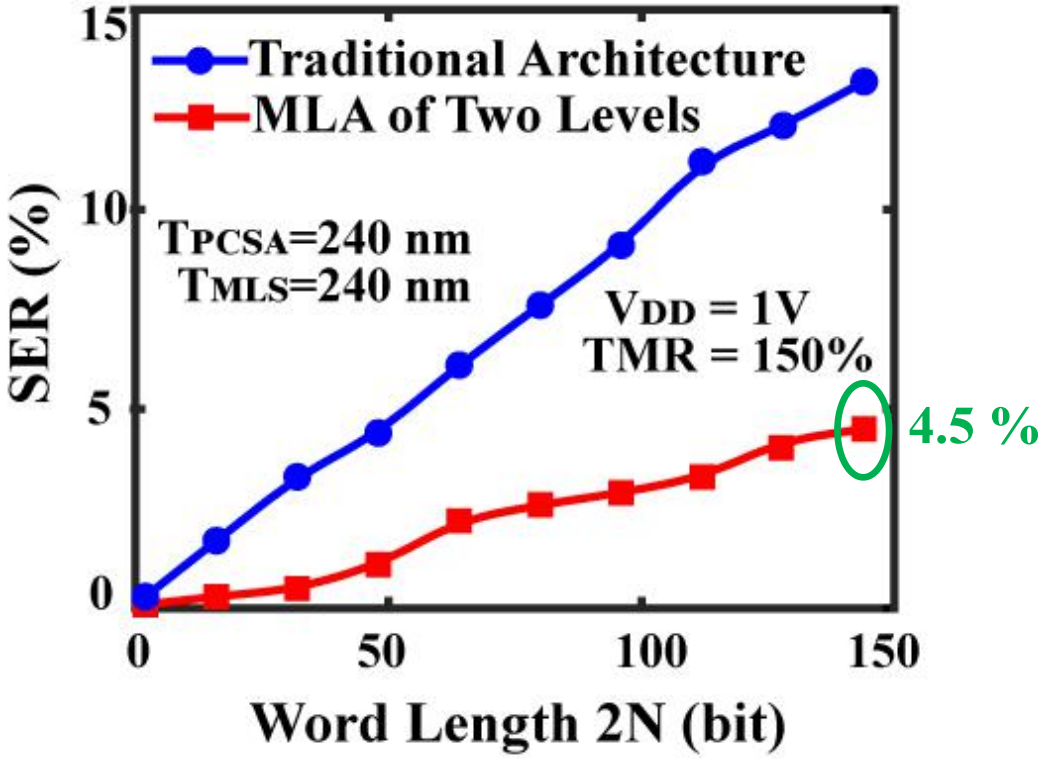
Proposed multi-level architecture (MLA)



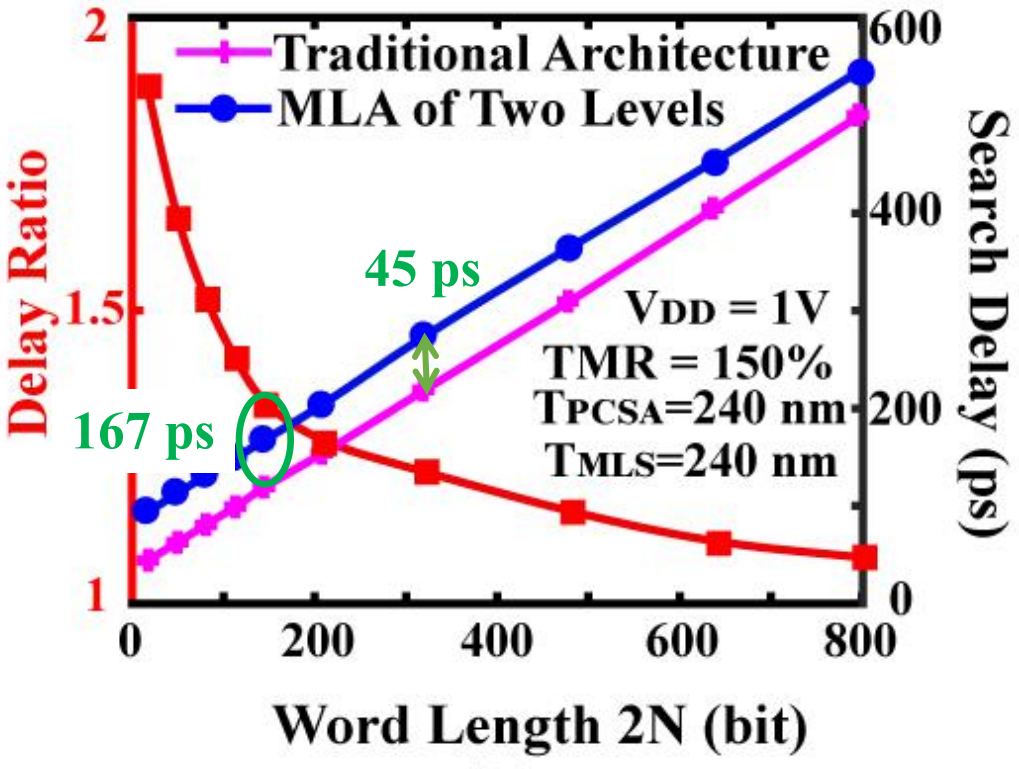
- ✓ Two levels
- ✓ Level I is matched, level II is performed
- ✓ Level I is mismatched, level II is idle

Schematic of a 4×2N NV-CAM in the proposed multi-level architecture (MLA)

Performance Evaluation

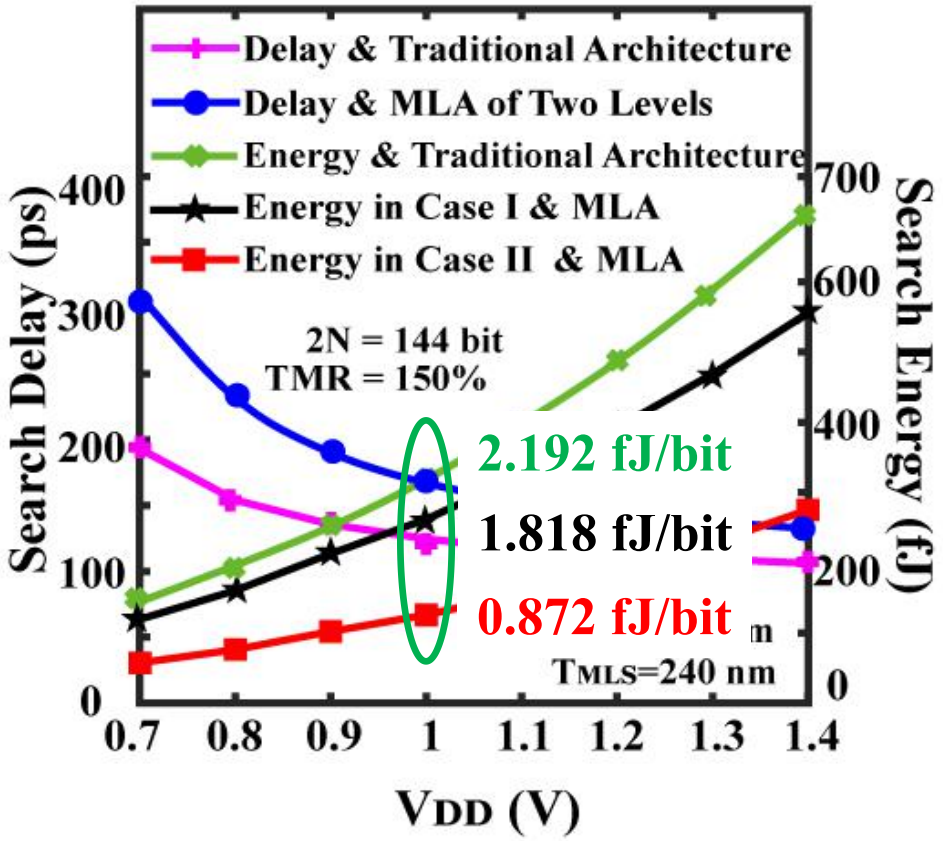


(a) SER with different word length



(b) Search delay and ratio with different word length

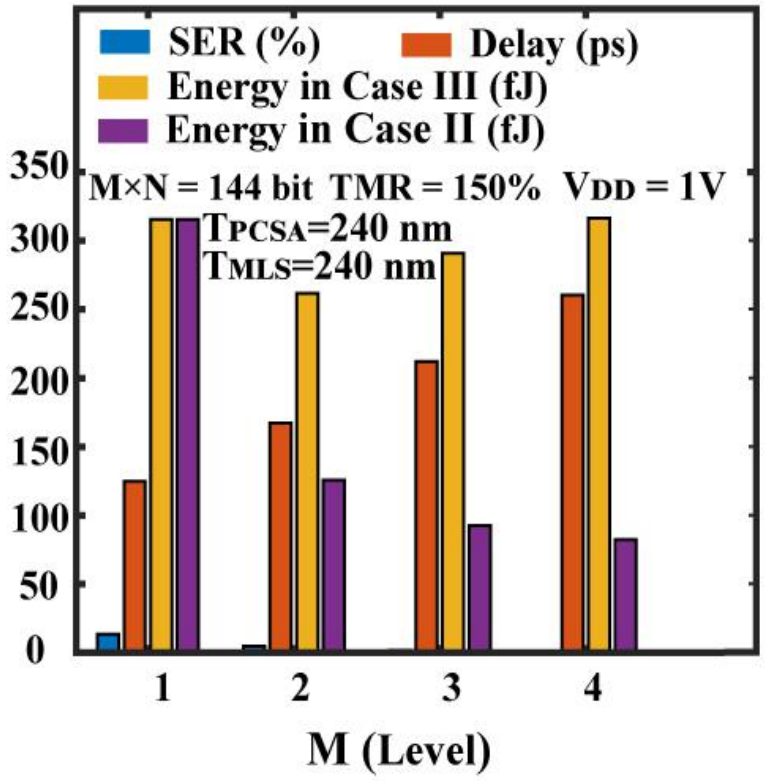
Performance Evaluation



(c) Search delay and energy with different V_{DD}

- ✓ **Case I:** 1-bit mismatch in level II
- ✓ **Case II:** 1-bit mismatch in level I
- ✓ **Case III:** Both levels match

➢ **Amount of transistors per bit: 11/M+3**

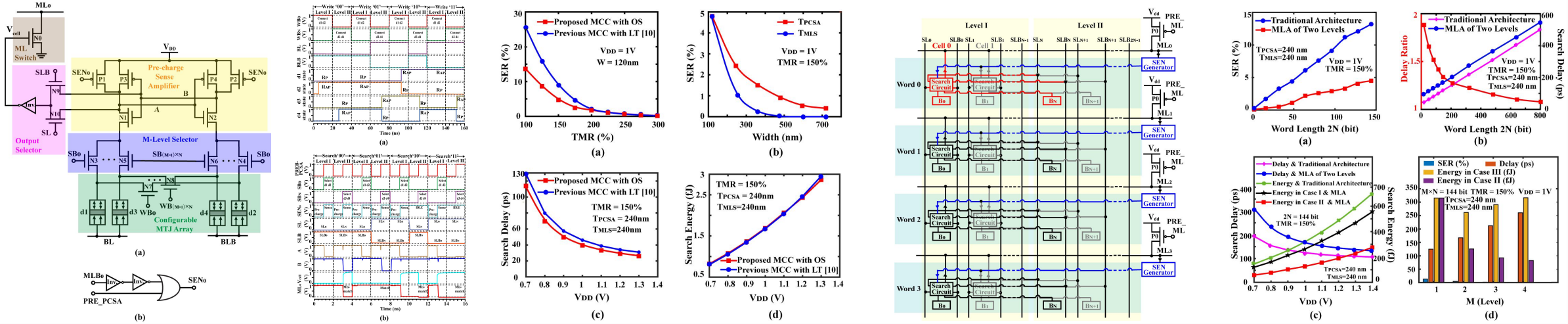


(d) Performance of a 1×144 NV-CAM with different M

Outline

Conclusion

- A **multi-context cell (MCC)** circuit by employing **an output selector (OS)** instead of a logic tree (LT)
  - Improve the reliability and bit search speed by reducing transistors' amount in discharge branches.
  - Improve the area efficiency by integrating multiple DMCs in one NV-CAM cell.
  - TMR, T_{PCSA}, T_{MLS} and V_{DD} are set to be 150 %, 240 nm, 240 nm and 1 V, respectively.
- A **SEN generator** to realize the **multi-level architecture (MLA)** for NV-CAM
  - Improve the reliability and word search energy by bringing inessential search operations to idle state.
  - The cost of search delay is little.
  - Improve the performance of NV-CAM by increasing levels' amount.



Thanks for your attention

Email：zy1902302@buaa.edu.cn
deming.zhang@buaa.edu.cn